ESD1524D3LIN

Description

ESD1524D3LIN in a very small SOD323 Surface-Mounted Device (SMD) plastic package designed to protect one automotive Local Interconnect Network (LIN) bus line from the damage caused by Electro Static Discharge (ESD) and other transients.

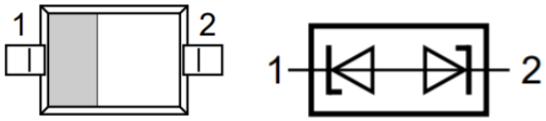
Features

- Package: SOD-323
- Ultra low leakage: nA level
- Working voltage: 15/24V
- Low clamping voltage
- Response Time is Typically < 1 ns
- Complies with following standards:
  IEC 61000-4-2 (ESD) immunity test
  Air discharge: ±30kV
  Contact discharge: ±30Kv
- AEC-Q101 qualified
- Marking code: 54

Applications

- LIN – bus protection
- Automotive applications

Circuit Diagram



Absolute Ratings

Tamb=25°C unless otherwise specified

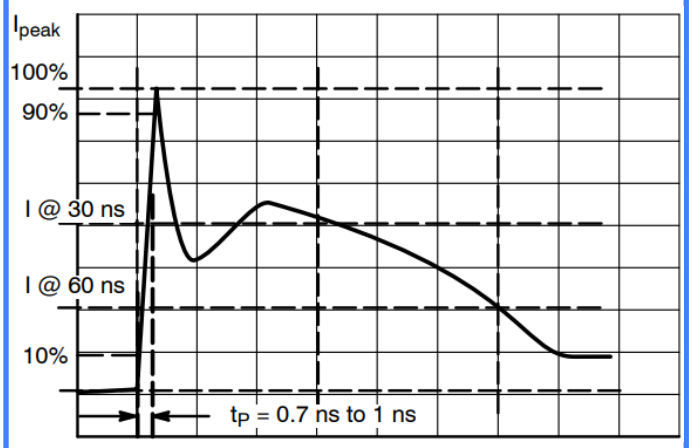
Parameter	Symbol	Value	Unit
Maximum Reverse Peak Pulse Current(8/20μS)	I_{PP}(pin1 to pin2) I_{PP}(pin2 to pin1)	8 5	A
ESD per IEC 61000−4−2 (Air)	V_{ESD}	±30	KV
ESD per IEC 61000−4−2 (Contact)		±30	
Storage Temperature Range	T_{STJ}	-55 to +150	℃
Operating Temperature Range	T_J	-40 to +125	℃

Electrical Characteristics

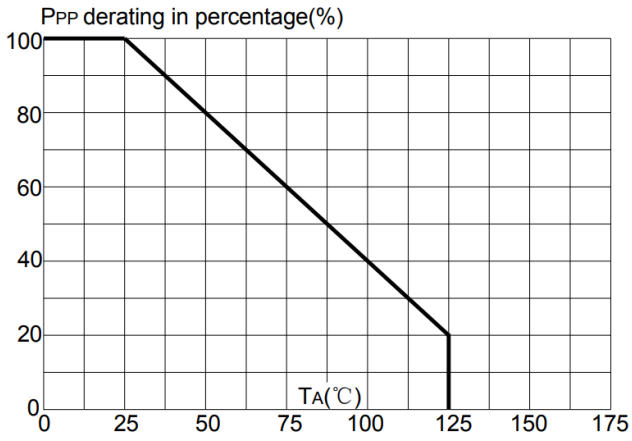
TA=25°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{RWM}	Reverse Working Peak Voltage	pin1 to pin2 pin2 to pin1			15 24	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA (pin1 to pin2) I_T = 1mA (pin2 to pin1)	16 26.5		19 30	V
I_R	Reverse Current	V_{RWM} =15V(pin1 to pin2) V_{RWM} =24V(pin2 to pin1)			0.1 0.1	μA
V_C	Clamping Voltage (t_P =8/20μs)	I_{PP}=8A(pin1 to pin2) I_{PP}=5A(pin2 to pin1)			35 51	V
C_D	Diode Capacitance	VR = 0V, f = 1MHz		30		pF

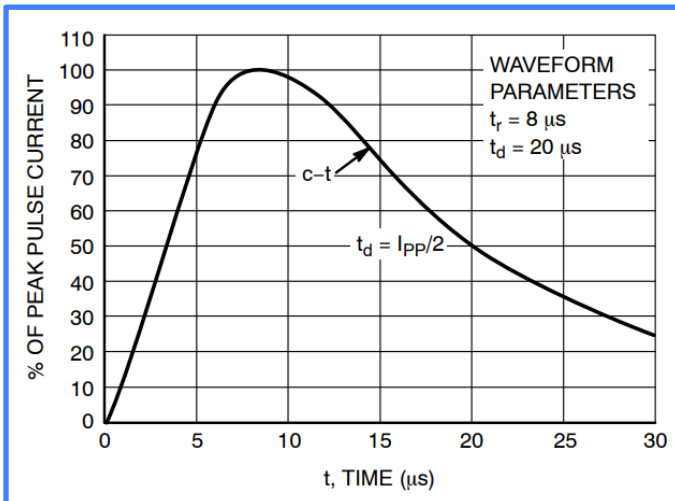
Characteristic Curves



IEC61000−4−2 Pulse Waveform

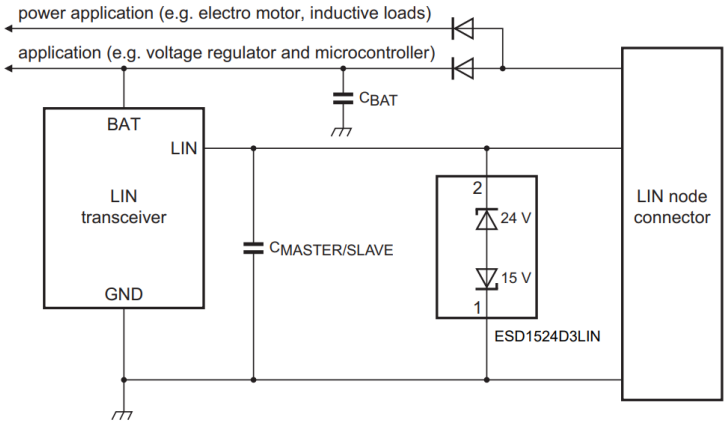


Power Derating Curve



8/20µs Pulse Waveform

Typical Applicatipn

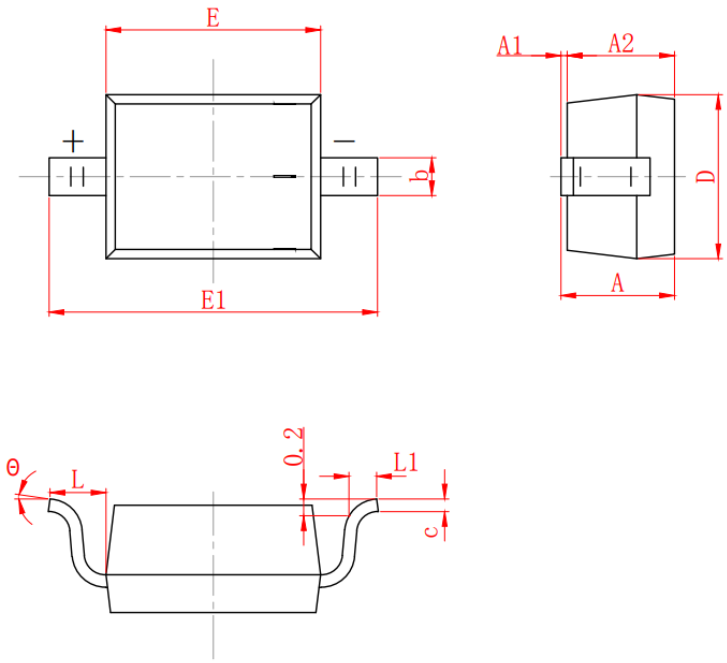


Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the ESD1524D3LIN as close to the input terminal or connector as possible.
2. The path length between the ESD1524D3LIN and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protection conductors in parallel with unprotected conductor.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias

SOD323 Package Outline & Dimensions



Symbol	Dimensions in mm	
	min	max
A		1.000
A1	0.000	0.100
A2	0.800	0.900
b	0.250	0.400
c	0.008	0.150
D	1.200	1.400
E	1.600	1.800
E1	2.300	2.700
L	0.475(REF)	
L1	0.250	0.400
θ	0°	8°

Disclaimer

Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.

Users should verify actual device performance in their specific applications.